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DLA PIPER RUDNICK GRAY CARY US, LLP
2000 UNIVERSITY AVENUE
E. PALO ALTO, CA 94303-2248

EXAMINER	
GOLDEN, JAMES R	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 04/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/800,349	SATO ET AL.	
	Examiner	Art Unit	
	James Golden	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12 March 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application 10/800349 has a total of 12 claims pending. There are 3 independent claims and 9 dependent claims.

Information Disclosure Statement

1. The information disclosure statement submitted on 03/12/2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

3. The disclosure is objected to because of the following informalities:

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet **within the range of 50 to 150 words**. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be

avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Appropriate correction is required.

Claim Objections

5. **Claims 1-12** are objected to because of the following informalities: "IP (intellectual property)" (claim 1, line 4; also used in claims 5 and 9) is not a term commonly understood in the art; claims 2-4, 6-8 and 10-12 are objected to because of their dependence on claims 1, 5 and 9, respectively. These objections can be overcome by correcting the term to one that is commonly understood in the art. Additionally, if acronyms ("IP", "TLB") are used in the claims, the full term should be written out in each independent claim.

6. **Claims 1-4 and 9-12** are objected to because of the following informalities: "a system memory and controls DMA (Direct Memory Access) transfer from the IP to the system memory" (claim 1, lines 3-5 and claim 9, lines 9-11) is not grammatically correct. These objections could be overcome by correcting the claims to read -- a system memory that controls DMA (Direct Memory Access) transfer from the IP to the system memory--.

7. **Claims 2-4, 6-8 and 10-12** are objected to because of the following informalities: the use of indefinite articles, as in "An apparatus" (claims 2-4), "A system" (claim 6), "An system" (claims 7-8) and "A method" (claims 10-12), make the claims ambiguous as to whether they are independent or dependent. If they are independent, they should be rewritten to include the limitations of the claims they reference; if they are dependent they should begin with definite articles referring to the apparatus, system or method of the parent claim, as in --The storage control apparatus of claim...--, --The control system of claim...-- or --The method-- .

8. Appropriate correction is required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless – (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. **Claims 9-10** rejected under 35 U.S.C. 102(b) as being anticipated by Amini et al. (US 5,966,728).

11. **With respect to claim 9**, Amini et al. disclose a method of controlling DMA transfer in a system comprising:

- a CPU connected to a host bus **("system bus" 76 connected to "processor complex" 14 through "memory bus" 30 of Fig. 1B; column 3, lines 60-64)**;

- at least one IP connected to one of the host bus and a peripheral bus **("I/O bus" 32 connected to "I/O devices" 28 of Fig. 1B; column 3, lines 55-57; note: an IP is interpreted as "a controller related to an external interface", as in page 1, lines 31-32 of applicant's background; an I/O device "serves as an interface", as in column 3, line 67 of Amini et al.)**;
- a system memory accessible by one of the CPU and the IP **(24 and 26 of Fig. 1B; column 3, lines 53-55, 60-64)**; and
- a storage control apparatus which is connected to the host bus, the peripheral bus, and the system memory **("memory controller" 58 of Fig. 1B and "bus interface unit" 64 of Figs. 1B and 3A)** and controls DMA transfer from the IP to the system memory **(column 5, lines 12-16)**,

comprising:

- judging whether an address given from one of the peripheral bus and the host bus indicates a memory area managed by the storage control apparatus in the system memory **(column 9, lines 33-49)**;
- when the address is in the memory area, judging on the basis of address information that indicates an area cacheable by the CPU whether the address given from one of the peripheral bus and the host bus indicates the area cacheable by the CPU **(column 9, line 67 -- column 10, line 12)**; and
- when it is judged on the basis of a judgment result that the CPU needs to be notified of the address, executing notification through the host bus **(column 10, lines 3-6)**.

12. **With respect to claim 10**, Amini et al. disclose an apparatus according to claim 9 (see above paragraph 11), wherein when said address judgment **("cache snooping logic" 114 of Fig. 3A)** section judges that the address indicates the cacheable area **(column 10, lines 3-6)**, said snoop address control section broadcasts a notification to invalidate cache data of the address onto the host bus **(column 10, lines 5-7)**.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. **Claims 1-2 and 5-6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Amini et al. (US 5,966,728) in view of Argade (US 6,223,255).

15. **With respect to claim 1**, Amini et al. disclose a storage control apparatus which is connected to a host bus connected to a CPU (Central Processing Unit) **("system bus" 76 connected to "processor complex" 14 through "memory bus" 30 of Fig. 1B; column 3, lines 60-64; note: an IP is interpreted as "a controller related to an external interface", as in page 1, lines 31-32 of applicant's background; an I/O device "serves as an interface", as in column 3, line 67 of Amini et al.)**, a peripheral bus connected to at least one IP (Intellectual Property) **("I/O bus" 32 of Fig. 1B connected to "I/O devices" 28; column 3, lines 55-57)**, and a system

memory **(24 and 26 of Fig. 1B; column 3, lines 53-55)** and controls DMA (Direct Memory Access) transfer from the IP to the system memory **(column 5, lines 12-16)**, comprising:

- an address map judgment section **("memory address compare logic" 110 of Fig. 3A, internal to 64 of Fig. 1B)** which judges whether an address given from one of the peripheral bus and said host bus indicates a memory area managed by said storage control apparatus in the system memory **(column 9, lines 33-49)**;
- a memory control section ("**memory controller" 58 of Fig. 1B;**) which controls data transfer to/from the system memory **(column 5, lines 12-16)**;
- an address judgment section **("cache snooping logic" 114 of Fig. 3A)** which judges on the basis of the address information whether the address given from one of the peripheral bus and the host bus indicates the area cacheable by the CPU **(column 9, line 67 -- column 10, line 12)**; and
- a snoop address control section **("cache snooping logic" 114 of Fig. 3A)** which, when it is judged on the basis of a judgment result from said address judgment section that the CPU needs to be notified of the address, executes notification through the host bus **(column 10, lines 3-7)**.

Amini et al. do not disclose the limitation further comprising:

- a TLB (Translation Look-aside Buffer) information holding section which holds address information that indicates an area cacheable by the CPU; and

- address information held by said TLB information holding section stores whether the address given from one of the peripheral bus and the host bus indicates the area cacheable by the CPU.

However, Argade disclose the limitation further comprising:

- a TLB (Translation Look-aside Buffer) information holding section which holds address information that indicates an area cacheable by the CPU **(column 7, lines 20-22)**; and
- address information held by said TLB information holding section stores whether the address given from one of the peripheral bus and the host bus indicates the area cacheable by the CPU **(column 7, lines 20-22)**.

Amini et al. and Argade are analogous art because they are from the same field of endeavor, namely memory access control.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the TLB data indicating whether memory is cacheable of Argade with the memory controller of Amini et al. The motivation for doing so would have been because the TLB allows for "faster translation" **(column 3, line 50)**.

Therefore, it would have been obvious to a person of ordinary skill in the art to combine Argade with Amini et al. for the benefit of a TLB data indicating whether memory is cacheable with a memory controller to obtain the invention as specified in claim 1.

16. **With respect to claim 2**, Amini et al. disclose an apparatus according to claim 1 (see above paragraph 15), wherein when said address judgment **("cache snooping**

logic" 114 of Fig. 3A) section judges that the address indicates the cacheable area **(column 10, lines 3-6)**, said snoop address control section broadcasts a notification to invalidate cache data of the address onto the host bus **(column 10, lines 6-12)**.

17. **With respect to claim 5**, Amini et al. disclose a control system capable of DMA transfer, comprising:

- a CPU connected to a host bus **("system bus" 76 connected to "processor complex" 14 through "memory bus" 30 of Fig. 1B; column 3, lines 60-64)**;
- at least one IP connected to one of the host bus and a peripheral bus **("I/O bus" 32 connected to "I/O devices" 28 of Fig. 1B; column 3, lines 55-57; note: an IP is interpreted as "a controller related to an external interface", as in page 1, lines 31-32 of applicant's background; an I/O device "serves as an interface", as in column 3, line 67 of Amini et al.)**;
- a system memory accessible by one of said CPU and said IP **(24 and 26 of Fig. 1B; column 3, lines 53-55)**; and
- a storage control apparatus which is connected to the host bus, the peripheral bus, and said system memory and controls DMA transfer from said IP to said system memory **(column 5, lines 12-16)**, said storage control apparatus comprising
    - an address map judgment section **("memory address compare logic" 110 of Fig. 3A, internal to 64 of Fig. 1B)** which judges whether an address given from one of the peripheral bus and the host bus indicates a

memory area managed by said storage control apparatus in said system memory **(column 9, lines 33-49)**,

- a memory control section which controls data transfer to/from said system memory **(column 5, lines 12-16)**,
- an address judgment section **("cache snooping logic" 114 of Fig. 3A)** which judges on the basis of the address information whether the address given from one of the peripheral bus and the host bus indicates the area cacheable by said CPU **(column 9, line 67 -- column 10, line 12)**, and
- a snoop address control section **("cache snooping logic" 114 of Fig. 3A)** which, when it is judged on the basis of a judgment result from said address judgment section that said CPU needs to be notified of the address, executes notification through the host bus **(column 10, lines 3-6)**.

Amini et al. do not disclose the limitation further comprising:

- a TLB information holding section which holds address information that indicates an area cacheable by the CPU; and
- address information held by said TLB information holding section stores whether the address given from one of the peripheral bus and the host bus indicates the area cacheable by the CPU.

However, Argade disclose the limitation further comprising:

- a TLB (Translation Look-aside Buffer) information holding section which holds address information that indicates an area cacheable by the CPU **(column 7, lines 20-22)**; and
- address information held by said TLB information holding section stores whether the address given from one of the peripheral bus and the host bus indicates the area cacheable by the CPU **(column 7, lines 20-22)**.

Amini et al. and Argade are analogous art because they are from the same field of endeavor, namely memory access control.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the TLB data indicating whether memory is cacheable of Argade with the memory controller of Amini et al. The motivation for doing so would have been because the TLB allows for "faster translation" **(column 3, line 50)**.

Therefore, it would have been obvious to a person of ordinary skill in the art to combine Argade with Amini et al. for the benefit of a TLB data indicating whether memory is cacheable with a memory controller to obtain the invention as specified in claim 5.

18. **With respect to claim 6**, Amini et al. disclose a system according to claim 5 (see above paragraph 17), wherein when said address judgment section **("cache snooping logic" 114 of Fig. 3A)** judges that the address indicates the cacheable area **(column 10, lines 3-6)**, said snoop address control section broadcasts a notification to invalidate cache data of the address onto the host bus **(column 10, lines 6-12)**.

19. **Claims 11-12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Amini et al. (US 5,966,728) in view of Carmon et al. (US 5,404,522).

20. **With respect to claim 11**, Amini et al. disclose an apparatus according to claim 9 (see above paragraph 11), wherein said snoop address control section has a storage section which stores addresses **(column 11, lines 28-35)**.

Amini et al. do not disclose the limitation wherein the snoop address control section burst-transfers the addresses to the host bus when the addresses corresponding to a burst size of the host bus are stored.

However, Carmon et al. disclose the limitation wherein the addresses are burst-transferred to the host bus when the addresses corresponding to a burst size of the host bus are stored **(column 15, lines 57-61; column 16, lines 34-50)**.

Carmon et al. and Amini et al. are analogous art because they are from the same field of endeavor, namely memory access control.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the burst transfer of Carmon et al. with the memory controller of Amini et al. The motivation for doing so would have been because data transfer bursts are "guaranteed to be met within the time interval prescribed" **(column 14, lines 6-7)**.

Therefore, it would have been obvious to a person of ordinary skill in the art to combine Carmon et al. with Amini et al. for the benefit of burst transfer of information to obtain the invention as specified in claim 11.

21. **With respect to claim 12**, Amini et al. disclose an apparatus according to claim 11 (see above paragraph 20). Amini et al. disclose the limitations wherein when

said address judgment **("cache snooping logic" 114 of Fig. 3A)** section judges that the address indicates the cacheable area **(column 10, lines 3-6)**, said snoop address control section broadcasts a notification to invalidate cache data of the address onto the host bus **(column 10, lines 6-12)**.

22. **Claims 3-4 and 7-8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Amini et al. (US 5,966,728) in view of Argade (US 6,223,255) as applied to claims 1-2 and 5-6 above (see paragraphs 15-18), and further in view of Carmon et al. (US 5,404,522).

23. **With respect to claim 3**, Amini et al. and Argade disclose an apparatus according to claim 1 (see above paragraph 15), wherein said snoop address control section has a storage section which stores addresses **(column 11, lines 28-35)**.

Amini et al. and Argade do not disclose the limitation wherein the snoop address control section burst-transfers the addresses to the host bus when a size of data indicated by the stored addresses has reached a burst size of the host bus.

However, Carmon et al. disclose the limitation wherein the addresses are burst-transferred to the host bus when a size of data indicated by the stored addresses has reached a burst size of the host bus **(column 15, lines 57-61; column 16, lines 34-50)**.

Carmon et al., Amini et al. and Argade are analogous art because they are from the same field of endeavor, namely memory access control.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the burst transfer of Carmon et al. with the memory controller of

Amini et al. The motivation for doing so would have been because data transfer bursts are "guaranteed to be met within the time interval prescribed" **(column 14, lines 6-7)**.

Therefore, it would have been obvious to a person of ordinary skill in the art to combine Carmon et al. with Amini et al. and Argade for the benefit of burst transfer of information to obtain the invention as specified in claim 3.

24. **With respect to claim 4**, Amini et al. and Argade disclose an apparatus according to claim 3 (see above paragraph 23). Amini et al. disclose the limitations wherein when said address judgment section **("cache snooping logic" 114 of Fig. 3A)** judges that the address indicates the cacheable area **(column 10, lines 3-6)**, said snoop address control section broadcasts a notification to invalidate cache data of the address onto the host bus **(column 10, lines 6-12)**.

25. **With respect to claim 7**, Amini et al. and Argade disclose an apparatus according to claim 5 (see above paragraph 17), wherein said snoop address control section has a storage section which stores addresses **(column 11, lines 28-35)**.

Amini et al. and Argade do not disclose the limitation wherein the snoop address control section burst-transfers the addresses to the host bus when the addresses corresponding to a burst size of the host bus are stored.

However, Carmon et al. disclose the limitation wherein the addresses are burst-transferred to the host bus when the addresses corresponding to a burst size of the host bus are stored **(column 15, lines 57-61; column 16, lines 34-50)**.

Carmon et al., Amini et al. and Argade are analogous art because they are from the same field of endeavor, namely memory access control.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the burst transfer of Carmon et al. with the memory controller of Amini et al. The motivation for doing so would have been because data transfer bursts are "guaranteed to be met within the time interval prescribed" **(column 14, lines 6-7)**.

Therefore, it would have been obvious to a person of ordinary skill in the art to combine Carmon et al. with Amini et al. and Argade for the benefit of burst transfer of information to obtain the invention as specified in claim 7.

26. **With respect to claim 8**, Amini et al. and Argade disclose an apparatus according to claim 3 (see above paragraph 23). Amini et al. disclose the limitations wherein when said address judgment **("cache snooping logic" 114 of Fig. 3A)** section judges that the address indicates the cacheable area **(column 10, lines 3-6)**, said snoop address control section broadcasts a notification to invalidate cache data of the address onto the host bus **(column 10, lines 6-12)**.

Conclusion

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Stracovsky (US 6,442,666) disclose a TLB information-holding section.
- Amini et al. (US 5,659,696) teach a similar DMA system to the DMA system of Amini et al. (US 5,966,728);
- Kelly et al. (US RE38,428) teach a memory controller with a snooping mechanism and access to different types of memory;

- Quach (US 5,659,709) teaches a memory controller with a snooping mechanism and cacheable and non-cacheable sections of memory; and
- Date et al. (US 6,499,076) teach a memory controller with access to different types of memory.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Golden whose telephone number is 571-272-5628. The examiner can normally be reached on Monday-Friday, 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James R. Golden
Patent Examiner
Art Unit 2187

JRG

Brian R. Peugh
Primary Examiner
AU 2187

April 18, 2006